IN THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the above-referenced application:

1. (Currently Amended) A metal-oxide-semiconductor (MOS) device, comprising:

a semiconductor layer of a first conductivity type;

a source region of a second conductivity type formed in the semiconductor layer;

a drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the source region;

a gate formed proximate an upper surface of the semiconductor layer and at least partially between the source and drain regions;

a buried lightly-doped drain (LDD) region of the second conductivity type formed in the semiconductor layer between the gate and the drain region, the buried LDD region being formed below at least a portion of the drain region and extending ~~spaced~~ laterally from the drain region to below at least a portion of the gate; and

a second LDD region of the first conductivity type formed in the buried LDD region and proximate the upper surface of the semiconductor layer, the second LDD region being self-aligned with a first alignment structure formed substantially concurrently with the gate in a same processing step, ~~and~~ the second LDD region being spaced laterally from the gate such that the gate is non-overlapping relative to the second LDD region.

2. (Original) The device of claim 1, further comprising a shielding structure formed proximate the upper surface of the semiconductor layer and at least partially between the gate and the drain region, the shielding structure being electrically connected to the source region, the shielding structure being spaced laterally from the gate and being substantially non-overlapping relative to the gate.

3. (Original) The device of claim 2, wherein the shielding structure is formed substantially concurrently with the gate.

4. (Original) The device of claim 2, wherein a first insulating layer under the gate and a second insulating layer under the shielding structure are formed of different thicknesses in comparison to one another.

5. (Original) The device of claim 1, wherein the device comprises a diffused MOS (DMOS) device.

6. (Original) The device of claim 5, wherein the device comprises a lateral DMOS (LDMOS) device.

7. (Original) The device of claim 5, wherein the device comprises a vertical DMOS device.

8. (Original) The device of claim 1, wherein the buried LDD region is formed in the semiconductor layer at a depth in a range from about 0.5 micron to about two microns, and the second LDD region is formed in the semiconductor layer at a depth in a range from about 0.05 micron to about 0.5 micron.

9. (Currently Amended) The device of claim 1, further comprising ~~an~~ a second alignment structure formed proximate the upper surface of the semiconductor layer and at least partially between the second LDD region and the drain region, wherein the drain region is self-aligned to a first edge of the second alignment structure and the second LDD region is self-aligned with a second edge of the second alignment structure such that the second LDD region is self-aligned with the drain region.

10. (Currently Amended) An integrated circuit including at least one metal-oxide-semiconductor (MOS) device, the at least one MOS device comprising:

a semiconductor layer of a first conductivity type;

a source region of a second conductivity type formed in the semiconductor layer;

a drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the source region;

a gate formed proximate an upper surface of the semiconductor layer and at least partially between the source and drain regions;

a buried lightly-doped drain (LDD) region of the second conductivity type formed in the semiconductor layer between the gate and the drain region, the buried LDD region being formed below at least a portion of the drain region and extending ~~spaced~~ laterally from the drain region to below at least a portion of the gate; and

a second LDD region of the first conductivity type formed in the buried LDD region and proximate the upper surface of the semiconductor layer, the second LDD region being self-aligned with a first alignment structure formed substantially concurrently with the gate in a same processing step, ~~and~~ the second LDD region being spaced laterally from the gate such that the gate is non-overlapping relative to the second LDD region.

11. (Original) The integrated circuit of claim 10, wherein the at least one MOS device further comprises a shielding structure formed proximate the upper surface of the semiconductor layer and at least partially between the gate and the drain region, the shielding structure being electrically connected to the source region, the shielding structure being spaced laterally from the gate and being substantially non-overlapping relative to the gate.

12. (Currently Amended) The integrated circuit of claim 10, wherein the at least one MOS device further comprises ~~an~~ a second alignment structure formed proximate the upper surface of the semiconductor layer and at least partially between the second LDD region and the drain region, wherein the drain region is self-aligned to a first edge of the second alignment structure and the second LDD region is self-aligned with a second edge of the second alignment structure such that the second LDD region is self-aligned with the drain region.

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Canceled)

23. (Canceled)

24. (Canceled)

25. (New) The device of claim 1, wherein the first alignment structure is removed after forming the second LDD region.

26. (New) The integrated circuit of claim 10, wherein the first alignment structure in the at least one MOS device is removed after forming the second LDD region.